Ocean Color Experiment v2

Electrical Design

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Data Rates

Readout Data Rate:

- Assume 144 channels per scan
- 30 μs Integration Period
- 14 bits each channel

⇒ **Readout Data rate ~** (102deg/360deg) (144 channels x 14 bits/channel)/30μs **~ 19.04Mbps**

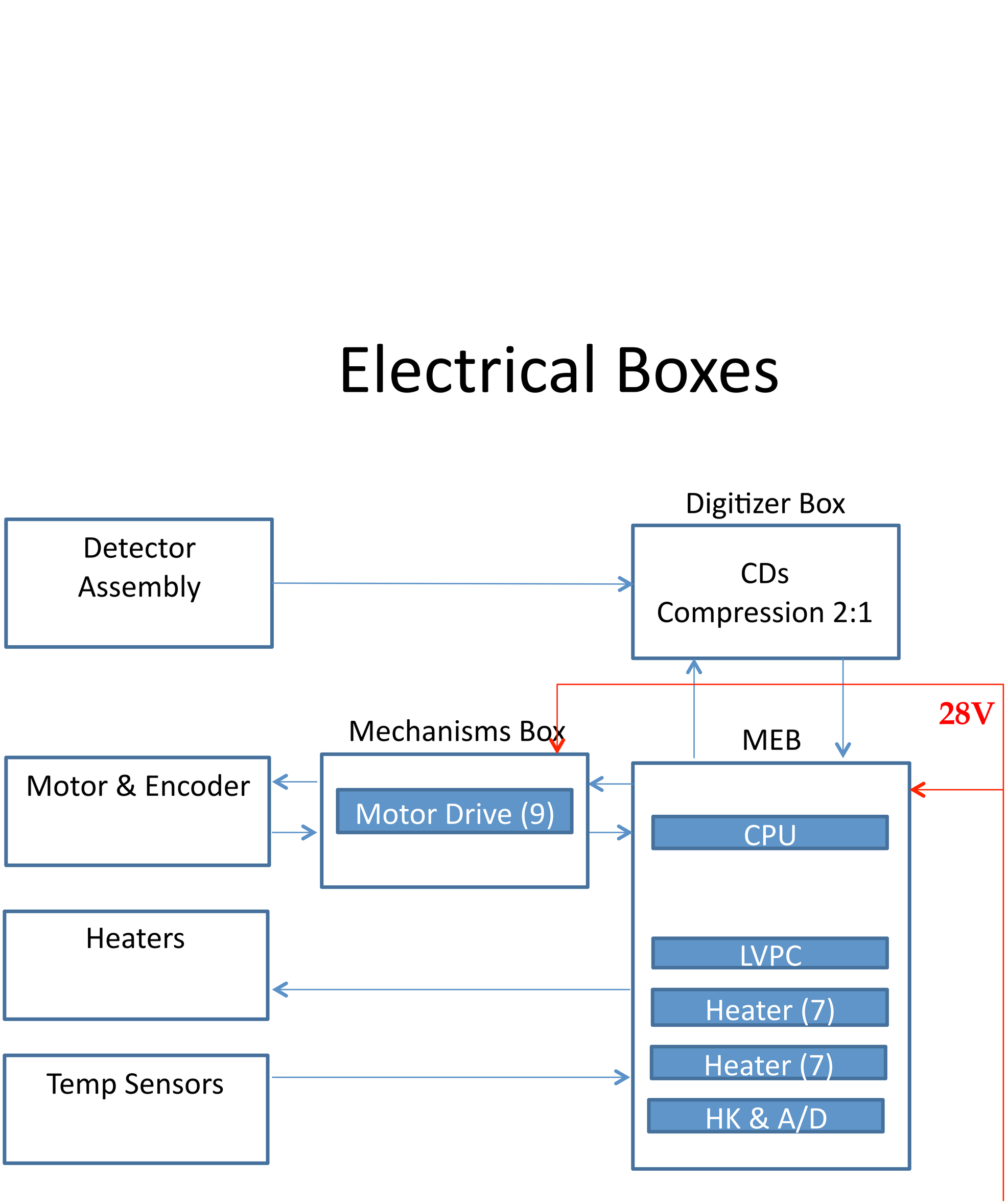
⇒ **Assume 50% for daylight only ~ 9.52Mbps** (avg.)

⇒ Assume data collection between **± 70deg** latitude

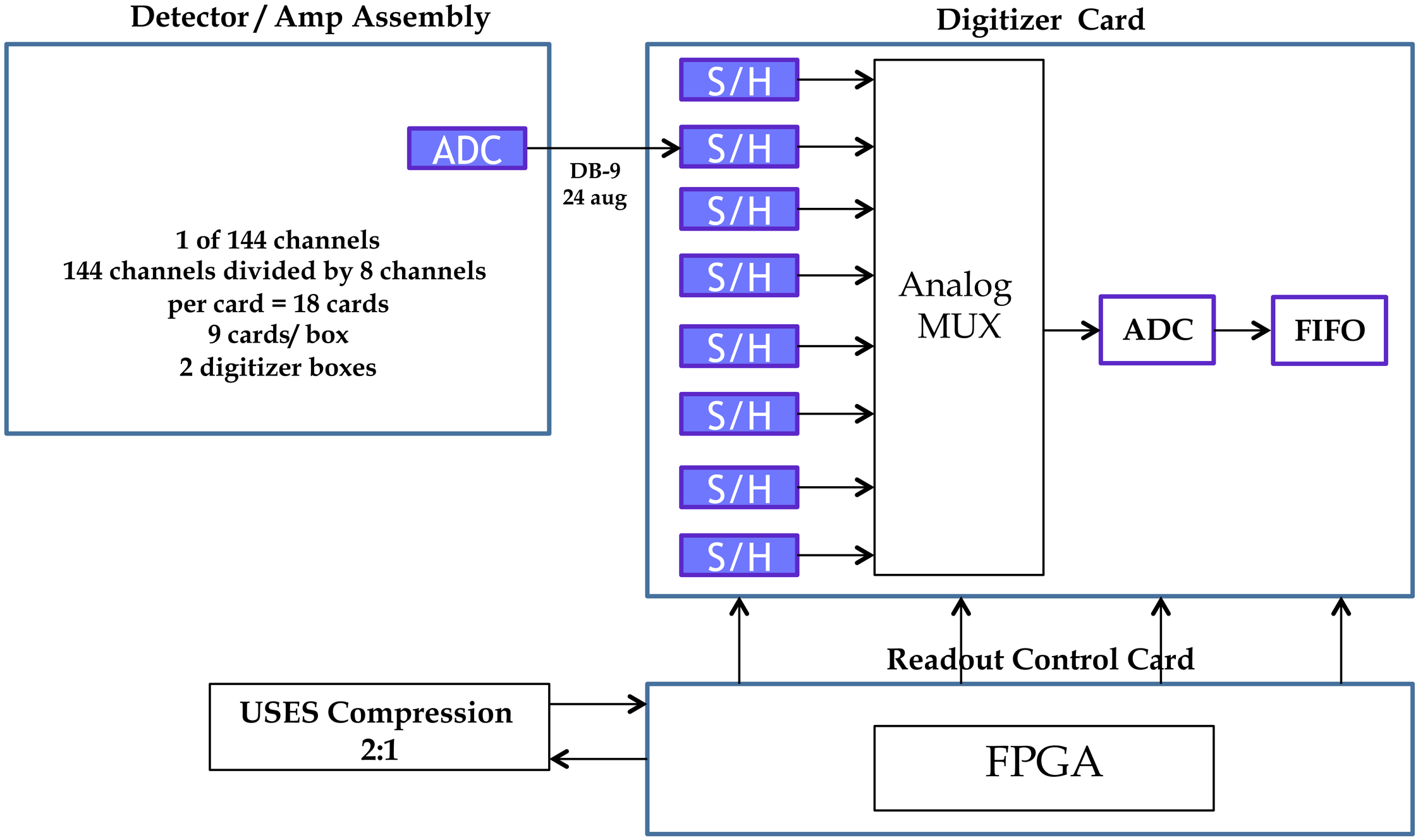
⇒ **Orbital Average Data Rate ~** 9.52Mbps x (140deg /180deg) **~ 7.4Mbps**

⇒ 7.4Mbps x (3600sec/hour) x 24hour/day = **639.36Gbits/day**

Electrical Boxes

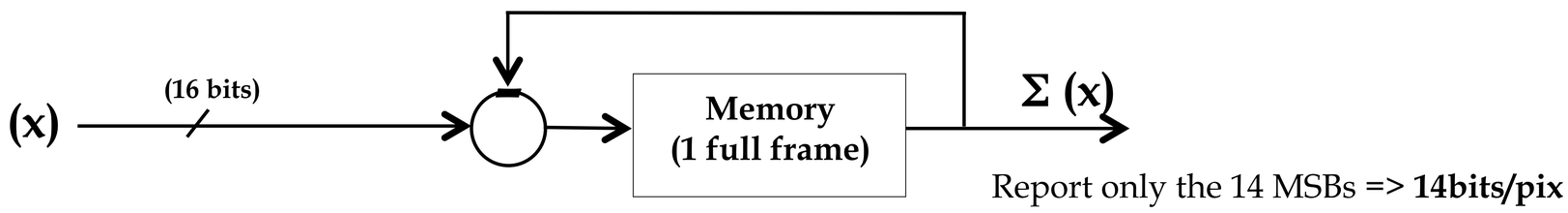


Digitizer Electronics



Correlated Double Sampling (CDS) Logic

Pixel CDS Algorithm



Correlated Double Sampling
Readout and store entire frame (144 pixels) at beginning of integration period, then readout entire frame at end of integration period, then subtract initial frame from final frame to produce a CDS frame.

Figure 3.

Mechanism Electronics

Baseline:

- Board-size is 6u
- Redundant windings and mechanism control for the scanning mechanism (not cross-strapped)
- Redundant mechanism control for the scanning mechanism (not cross-strapped)
- Redundant operational and survival heaters, thermostats, and control circuits

Mechanism Box

- Scanning Mechanism 1
- Scanning Mechanism 2
- Half-angle Mirror Mechanism 1
- Half-angle Mirror Mechanism 2
- Momentum Compensation Mechanism 1
- Momentum Compensation Mechanism 2
- Tilt Mechanism Motors 1
- Tilt Mechanism Motors 2
- Sun Calibration Mechanism

MEB Power

E-Box External Load	Power (W)
Detector and Amp Dissipation	145.0
Digitizer Electronics	82.0
Motors/Actuators (Scan Tel (12W avg), HAM (4W avg), Mom Comp (42W avg)	58.0
Mechanism Control (Scan Telescope, HAM, Mom Comp)	15.0
E-Box External Dissipation:	300.0
E-Box Boards	Power (W)
CPU Board + H/K	7.5
Thermal Control	28.0
E-Box Boards Dissipation:	35.5
E-Box Power Board Load	335.5
Converter % Efficiency	75
E-Box Converter Dissipation:	111.8
E-Box Dissipation:	147.3
Spacecraft Load	Power (W)
Additional Load(Tilt Mech & Cal Mech (30W pk, 0W avg):	0.0
Instrument Total:	447.3

Digitizer Card Power Calculations

- Sample n Hold = 135mW x 8 = 1080mW
- MUX = .01uW
- ADC = 1W
- FIFO = 2.5W
- Total per card = 4.5W per card
- 9 cards per box
- 2boxes
- Total per box = 41W
- Total Digitizing Power = 82W

Mechanisms Box Power

- **Motors/Actuators:**
  - Scan Tel (12W avg),
  - HAM (4W avg),
  - Mom Comp (42W avg)
- **Total:**
  - 58W

Box Size

- All boxes are 6u
- 5 cards in MEB
- 9 cards in 2 Digitizer Boxes
- 9 cards in Mechanisms Box

MEB Size

CCE Circuit Boards			Comments
Length	Width	Quantity	
8	6	5	Length/Width in inches
20.32	15.24		Length/Width in centimeters (1in = 2.54 cm)
Backplane:			
8	5	0.4	Backplane Length/Width in inches, Mass in Kg.
Board Mass Total:	2.9	Kg	My Metric: 0.5 Kg each 8"x6" board
	6.4	lbs	1lb = 0.45359237 Kg, 1Kg =2.204Kg
			1 in = 0.0254 meters = 2.54cm = 25.4 mm, 1 meter = 39.370 in
Electronics Box			
Depth (D)	Height (H)	Width (W)	
9	7	6	
22.86	17.78	15.24	(centimeters). Divide by 100 for meters
Surface Area Total	0.21		Area = 2(DH+HW+WD)/10000 square meters
Wall thickness (mm)	2.50		millimeters. Divide by 1000 for meters
Density (Aluminum)	2,700.00		Kg/Meter3
Housing Mass:	1.4	Kg	(Mass = Volume x Density. ie Area x Thickness x Density)
	3.1	lbs	
Box Mass Total:	4.3	Kg	(ie. C8+C19)
	9.5	lbs	(ie. C9+C20)

Digitizer and Mechanisms Boxes Size

CCE Circuit Boards			Comments
Length	Width	Quantity	
8	6	9	Length/Width in inches
20.32	15.24		Length/Width in centimeters (1in = 2.54 cm)
Backplane:			
8	9	0.8	Backplane Length/Width in inches, Mass in Kg.
Board Mass Total:	5.3	Kg	My Metric: 0.5 Kg each 8"x6" board
	11.6	lbs	1lb = 0.45359237 Kg, 1Kg =2.204Kg
			1 in = 0.0254 meters = 2.54cm = 25.4 mm, 1 meter = 39.370 in
Electronics Box			
Depth (D)	Height (H)	Width (W)	
9	7	10	
22.86	17.78	25.4	(centimeters). Divide by 100 for meters
Surface Area Total	0.29		Area = 2(DH+HW+WD)/10000 square meters
Wall thickness (mm)	2.50		millimeters. Divide by 1000 for meters
Density (Aluminum)	2,700.00		Kg/Meter3
Housing Mass:	1.9	Kg	(Mass = Volume x Density. ie Area x Thickness x Density)
	4.3	lbs	
Box Mass Total:	7.2	Kg	(ie. C8+C19)
	15.9	lbs	(ie. C9+C20)

Backup Charts

Main Electronics Box (MEB) Summary

Circuit Boards (20x15) cm² (8”x6”), 0.5Kg each	QTY	PWR (Watts)	Mass (Kg)	Description	% Analog /Digital
Power Switching Card	1	5.0	0.5		70/25
Single Board Computer	1	10.0	0.5		5/90
Digital I/O Card	1	5.0	0.5		5/90
Stepper Motor Drive Card	1A/1B	3.0	1.0		70/25
Housekeeping	1	4.0	0.5		50/50
Power Converter	1	9.7	0.5	Assume 75% efficiency	90/5
Backplane	1	-	0.7		
Housing	1	-	1.7		
Total	**-**	**36.7**	**5.9**		

Box Size: (23x18x20) cm³, or (10” X 7” x 13”), 5.9Kg (ie. 4.2Kg board total + 1.7 Kg Housing)

Harness Mass Estimates

		Harness							Wrapper		Connector Mass		Backshell Mass		Line Totals
						Length	Density	Mass	Density	Mass	From	To	From	To	Mass
From	To	Type	Description	Qty	Meters	(ft.)	(g/ft.)	(g)	(g/ft.)	(g)	(g)	(g)	(g)	(g)	(g)
FEE Box	Detector	TSP	analog (24 AWG)	252	1.0	3.3	5.600	4629.92	5.200	17.06	41.200	0	68.000	0	4756.18
FEE Box	DEEP Box	TSP	signal, address (24AWG)	252	2.0	6.6	5.600	9259.84	5.200	34.12	41.200	41.200	68.000	68.000	9512.36
MEB	FEE Box	Pair	power (20AWG)	8	2.2	7.2	5.000	288.71	5.200	37.53	7.600	7.600	21.000	21.000	383.45
MEB	DEEP Box	Pair	power (20AWG)	1	0.2	0.7	5.000	3.28	5.200	3.41	5.600	5.600	15.000	15.000	47.89
MEB	DEEP Box		1553	1	0.2	0.7	7.200	4.72	5.200	3.41	5.600	5.600	15.000	15.000	49.34
MEB	FW & X-Ray Source	Pair	HV power	1	1.0	3.3	5.000	16.40	5.200	17.06	5.600	5.600	15.000	15.000	74.66
MEB	FW & X-Ray Source		1553	1	1.0	3.3	7.200	23.62	5.200	17.06	5.600	5.600	15.000	15.000	81.88
MEB	ADR Electronics	Pair	power (20AWG)	1	3.0	9.8	5.000	49.21	5.200	51.18	5.600	5.600	15.000	15.000	141.59
MEB	ADR Electronics		1553	1	3.0	9.8	7.200	70.87	5.200	51.18	5.600	5.600	15.000	15.000	163.25
MEB	Cryo Electronics	Pair	power (20AWG)	1	1.0	3.3	5.000	16.40	5.200	17.06	5.600	5.600	15.000	15.000	74.66
MEB	Cryo Electronics		1553	1	1.0	3.3	7.200	23.62	5.200	17.06	5.600	5.600	15.000	15.000	81.88
MEB	3X (Heaters A/B)	TP	power (20AWG)	6	3.0	9.8	5.000	295.28	5.200	51.18	7.600	7.600	21.000	21.000	403.66
MEB	3X (Temp Sens - A/B)	TP	analog (22AWG)	6	3.0	9.8	3.200	188.98	5.200	51.18	7.600	7.600	21.000	21.000	297.36
MEB	2X (actuator - A/B)	TSP	power (20AWG)	4	1.5	4.9	5.000	98.43	5.200	25.59	7.600	7.600	21.000	21.000	181.22
ADR	ADR Electronics	TP	analog	1	2.0	6.6	5.600	36.75	5.200	34.12	5.600	5.600	15.000	15.000	112.07
Cryocooler	Cryo Electronics A/B	TP	analog	2	2.0	6.6	5.600	73.49	5.200	34.12	5.600	5.600	15.000	15.000	148.81
								15079.5							
						Column Totals:		15079.53		462.34	168.8	127.6	370	302	16510.26 g
													Harness Total:		16.51 Kg

Predefined Schema for Costing New FPGA Developments

FPGA Development Cost Information

- **Predefined schema for costing new FPGA development**
  - Parametric cost estimate includes the procurement costs for flight selected FPGAs from the manufacturer; NRE cost estimate includes the engineering labor to generate the algorithms
- **The most used FPGA on future missions is the Actel AX-2000**
- **Many functions/algorithm that have been previously designed and coded, and are available as intellectual Property (IP) in VHDL Format. Implementing VHDL IP into an FPGA requires very little FTEs.**
  - IP developed by NASA is available for free
  - IP from industry requires a license for its usage
  - Examples of VHDL IP that are available
    - Spacewire Data Network Protocol/interface
    - PCI Data Bus Interface for both Bus Controller and Terminals
    - Mil-STD-1553 Data Bus Controller and Remote Terminals
    - Short Reed-Solomon Encoder/Decoder for Error Detection & Correction (EDAC) of Data in SEU vulnerable memory
    - Rice Data Compression Algorithm (~2:1 Lossless)
    - Pixel-Processor (for science data reduction)
    - Downlink Formatting & Encoding
      - CCSDS VCDU protocol Formatting
      - Long Reed-Solomon Encoding for EDAC across downlink channels
      - Convolution Encoding
      - Randomization

FPGA Firmware Development Costs

Unique FPGAs	Box	Algorithm Type	Cost
2 FPGAs	DEEP	Spacecube 2.0 Processor Card	(Included)
		Event Trigger	$400K
		Pulse Event Processing	$400K
		Data Reduction	$400K
		Total firmware development costs	**$1.2M**

FPGA Firmware Costing Scheme

- **This scheme was revised by several Product Design Leads (PDLs) in Code 564 in Oct, 2011 for the IDL to capture the firmware development labor associated with FPGAs**
  - The hardware costs are captured parametrically
- **$400K Minimum for FPGA Development for the chip pin assignments and interface frame work, for each unique FPGA (firmware costs are assumed to be zero for identical FPGA chips)**
  - 1.50 FTEs of New Code Design (VHDL coding and Simulation)
  - 0.50 FTEs of New Code Verification (by Analysis)
  - 0.25 FTEs of Signal Integrity Analysis (of all I/O lines)
  - 0.25 FTEs of Lab Code Test
- **$400K per unique Algorithm, which are executed from within the FPGA frame work**
  - 1.00 FTEs of New Algorithm
  - 1.00 FTEs of New Algorithm lab Test/Verification

FPGA Contacts at Goddard

Integrated Design Capability / Instrument Design Laboratory

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Issues / Conclusion

- No electrical tall poles or low TRL concerns.

- Design assumes separate pre-amplifier electronics, power supply, and data processing FPGAs for each half of the detector, thereby providing some degree of fault tolerance to meet the assumed three (3) year reliability goal.

- Baseline design utilizes Spacecube 2.0 which give superior performance for throughput (5000 MIPS), power @ 10W, and overall size/mass for the processor Card (and hence the DEEP Box). The DEEP Box will require custom designed DE Cards, modified I/O card, and modified LVPC, but will utilize standard processor card.

- Design drivers are the A/D converters and the DACs due to their large quantity (ie. This causes a multiplying effect for power consumption).

- The Main Electronics Box assumes purchased items only with no custom designed circuit boards to minimize cost.

- All heaters, motors, and actuators have redundant circuitry.

- Mass and power estimates are best estimates of actual (ie. no margin added)